FOWLER – NORDHEIM TUNNELING IN STRUCTURES WITH ULTRATHIN DIELECTRICS

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UDC 621.382

‰ 2001

Currents through ultrathin dielectric films SiO_2 are used for storage and erase charge in electrically programmable memory elements and are very important for reliability of ultra-large integral circuits (IC). The influence of different parameters such as the doping level and type of a substrate, oxide thickness, and post-metallization annealings is investigated in detail. MOS structures with aluminum gate were used for study. The doping level in substrates influences the Fowler – Nordheim current significantly, and this influence is decreased with a growth of the oxide thickness. The annealings in hydrogen and in H_2O reduce the Fowler – Nordheim current. The influence of H_2O is stronger. To explain the observed experimental results, the influence of the charge in SiO_2 on experimental current-voltage $I(V)$ characteristics and the corresponding Fowler – Nordheim curves of MOS structures is considered. The charge at the Si–SiO_2 interface and in SiO_2 was determined by step-by-step etching of silicon dioxide and measurements of capacitance-voltage $C(V)$ characteristics. The influence of the charge built-up in SiO_2 on the $I(V)$ characteristics of a MOS structure is based on the oxide charge induced tunnel transparency modification. The Fowler – Nordheim currents in MOS structures were theoretically calculated in the Wenzel – Kramers – Brillouin energy barrier transparency approximation.

Introduction

The continuing devices miniaturization in CMOS technology and corresponding gate oxide thickness scaling for these deep sub-micron transistors cause the use of thinner dielectric films in IC elements. Ultrathin oxides with high reliability are required for ultra-large IC applications. On the other hand, the tunneling of charge carriers through thin dielectric films is the important process in electrically erase programmable read-only memory (EEPROM) [1]. The influence of different technology parameters such as substrate and gate materials, substrate doping, post-gate thermal cycling, ets., is critical to achieve the optimum device performance and device reliability. The properties of SiO_2 films are changed with thickness reduction. Thermal oxidation at low temperatures (≤ 900 °C) causes a rise of the sufficient mechanical stress in the Si–SiO_2 system and, as a result, the changing of SiO_2 properties [2 – 4].

In this paper, we present the results of investigation of tunnel currents through ultrathin (4 – 9 nm) SiO_2 films and the influence of the concentration and type of doping impurities in a substrate and post-metallization annealing on tunneling. To minimize and explain the discrepancy among experimental and calculated data and scattering of experimental Fowler – Nordheim curves, the built-in charge into SiO_2 and its distribution are taken into account. For the analysis of experimental results, the simplified Fowler – Nordheim expression is used:

$$\ln\left(\frac{J}{E^2}\right) = A - \frac{B}{E}, \tag{1}$$

where J is the current density, E is the electric field strength in oxide,

$$E = \frac{V_g - \Phi_{ms}}{d_{\text{ox}}}, \tag{2}$$

where V_g is the gate electrode voltage, Φ_{ms} is the difference of the silicon and gate electrode work functions, d_{ox} is the oxide thickness. The pre-exponential factor A and the slope B are given in the classical FN theory by [4, 5]

$$A = \ln\left(\frac{q^3 m}{16\pi^2 \hbar m_{\text{ox}} \Phi_b}\right), \tag{3}$$

and

$$B = \frac{4}{3}\frac{\sqrt{2m_{\text{ox}}\Phi_b^3}}{q\hbar}, \tag{4}$$

where q is the electron charge, m and m_{ox} are the electron mass in free space and the forbidden band gap of oxide, respectively (here, $m_{\text{ox}} = 0.42\ m$), $2\pi\hbar$ is Planck's constant, and Φ_b is the barrier height in eV. According to [6], the image force correction can be omitted. The values A are got by extrapolation of Fowler – Nordheim curves to $1/E = 0$ and those of B from the slope of plots.

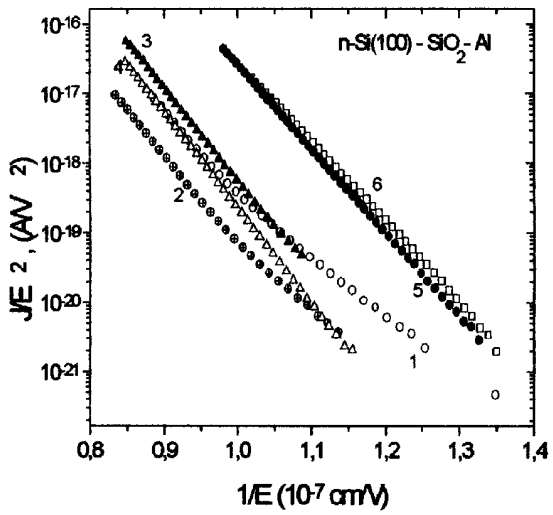

Fig. 1. Fowler – Nordheim plots of a MOS structure with different substrate doping level and SiO_2 thickness. Injection from substrate. *1* – $N_d = 2 \cdot 10^{14}$ cm^{-3}, $d_{ox} = 4.4$ nm; *2* – $N_d = 9.2 \cdot 10^{14}$ cm^{-3}, $d_{ox} = 4.4$ nm; *3* – $N_d = 2 \cdot 10^{14}$ cm^{-3}, $d_{ox} = 6.2$ nm; *4* – $N_d = 9.2 \cdot 10^{14}$ cm^{-3}, $d_{ox} = 6.2$ nm; *5* – $N_d = 2 \cdot 10^{14}$ cm^{-3}, $d_{ox} = 8.5$ nm; *6* – $N_d = 1.45 \cdot 10^{20}$ cm^{-3}, $d_{ox} = 8.1$ nm

1. Experiment

In this work, ultrathin (4 – 9 nm) gate oxide layers were grown on clean Si wafers by thermal oxidation in a conventional furnace. At the beginning, after the conventional (RCA) cleaning, sacrificial oxide films 80 – 100 nm were grown on silicon wafers at 1000 ℃ in O_2 with the following annealing in N_2 for 10 min at the oxidation temperature. The load and unload temperatures were 850 ℃ and the rates about 15 cm/min. Then these films were removed in an HF solution. A stable hydrogen passivated Si surface is obtained after etching the oxide layer by a diluted HF and rinsing in water [7]. The silicon wafers used were 100 mm in diameter with (100) and (111) orientations. The doping levels of *n*-Si substrates were equal to $2 \cdot 10^{14}$ and $9.2 \cdot 10^{14}$ cm^{-3}, *p*-Si substrates – $3.5 \cdot 10^{14}$ and $1.4 \cdot 10^{15}$ cm^{-3}. The higher doping concentrations of upper Si layers ($1.45 \cdot 10^{20}$ cm^{-3} for *n*-Si and $3.2 \cdot 10^{19}$ cm^{-3} for *p*-Si) were obtained by ion implantation of some substrates with As^+ ($E = 100$ keV, $D = 1000$ μC/cm^2) and B^+ ($E = 40$ keV, $D = 200$ μC/cm^2), correspondingly. After the ion implantation, the annealing at 1000 ℃ during 10 min in nitrogen was fulfilled. The doping was performed before the gate oxidation. Wafers of various types were simultaneously oxidized in the furnace. Thermal oxidation was done in dry O_2 under different conditions. The oxide thickness was determined by laser ellipsometry ($\lambda = 632.8$ mn) at 5 points spread over a wafer.

To investigate electron injection from the Si substrate and aluminum, MOS capacitors were fabricated on the *n*- and *p*-type of silicon wafers. Gates were received by magnetron sputtering of Al+1% Si. The definition of gate areas was performed by the standard lithographic processing. Post-metallization anneals, if applied, were provided by heating for 30 min in H_2 at 450 ℃ or in H_2O at 400 ℃. The areas of MOS capacitors were in the range from $1 \cdot 10^{-4}$ to $3 \cdot 10^{-4}$ cm^{-2}. Current-voltage curves were measured by applying a stepped voltage to the device and recording the gate current on a Hewlett Packard analyzer 4145A. The polarity of the measurement was chosen so that the silicon-oxide interface was driven in accumulation. The applied voltage was increased by 0.05 V steps until the electric breakdown of oxide.

2. Results and Discussion

2.1. Influence of Oxide Thickness and Substrate Doping Level

In these experiments, ultrathin oxide films were grown at 900 ℃ in dry O_2. The technological process included such subsequent steps: the load in a furnace at 900 ℃ in nitrogen, the annealing at 1000 ℃ in N_2 during 30 min, oxidation at 900 ℃ in oxygen, the annealing at 1050 ℃ in N_2 during 15 min and the unload at 900 ℃ in N_2.

Electron injection from substrate. The current-voltage characteristics in Fowler – Nordheim plots in the case of injection from the substrate (*n*-type Si) are presented in Fig. 1. The oxide thickness and substrate doping level are the parameters although substrate doping levels were taken into account by using Φ_{ms} in the electric field calculation ($\Phi_{ms} = f(N_{d,a})$) [8]. The dependences on doping levels are observed for all values of the oxide thickness. In the plot, it corresponds to a shift of curves for different doping levels at the same thickness. The maximum shift is observed for the thinner oxide thickness. A growth of the oxide thickness reduces the shift and the influence of doping is minimum at the oxide film thickness $d = 8.5$ nm.

The electron energy barriers at the Si–SiO_2 interface determined from the slopes of Fowler – Nordheim plots are presented in Table. The maximum values of Φ_b are observed at the oxide film thickness $d = 6.2$ nm. At the film thickness $d = 8.5$ nm, the dependence of Φ_b on doping level is slight.

Electron injection from gate. The electron energy barriers at the Al–SiO_2

interface are calculated from Fowler – Nordheim plots and shown in Table. In the case of electron injection from the Al gate, the current-voltage characteristics are placed closer to each other. This points out the less influence of a substrate doping level. But, at the oxide thickness $d = 4.4$ nm, the shift of curves is essential. The increase of the substrate doping level to $3.2 \cdot 10^{19}$ cm^{-3} causes a reduction of the curve slope.

The influence of the substrate doping level on the shifts and slopes of current-voltage characteristics is decreased with a growth of the oxide thickness from 4.4 to 8.5 nm for both types of silicon. But the increase of the doping level by some orders with ion implantation causes a change in electron energy barrier heights (at the oxide film thickness ~ 8 nm). The influence of boron doping on the barrier height is stronger than arsenic doping (Table). Direct tunneling was observed only in the case of *p*-type silicon.

To estimate the substrate doping level influence on electron tunneling, the redistribution of doped impurities between silicon and the oxide film during thermal oxidation was calculated using a program for modelling technoligical processes (SUPREM-3). The boron segregation into oxide is observed. The boron concentration in oxide is of the same order as that in substrate, but the phosphorus and arsenic concentrations into SiO_2 are lower by one order.

Under oxide growth at $T \leq 900$ °C, the essential intrinsic stress occurs into SiO_2 [2 – 4]. The stress influences SiO_2 film properties [4, 9]. It causes a nonuniform built-in charge distribution, that influences

Energy barrier heights deduced from Fowler – Nordheim curve slopes. Influence of the SiO_2 thickness, doping impurity, and doping level

n-Si(100)					
$N_d = 2 \cdot 10^{14}$ cm^{-3}, phosphorus		$N_d = 9.2 \cdot 10^{14}$ cm^{-3}, phosphorus		$N_d = 1.45 \cdot 10^{20}$ cm^{-3}, arsenic	
d_{ox}, mn	Φ_b, eV	d_{ox} nm	Φ_b, eV	d_{ox}, nm	Φ_b, eV
4.4	3.24	4.4	3.33	–	–
6.2	3.37	6.2	3.52	–	–
8.5	3.18			8.1	3.12
p-Si(100)					
$N_a = 3.5 \cdot 10^{14}$ cm^{-3}, boron		$N_a = 1.4 \cdot 10^{15}$ cm^{-3}, boron		$N_a = 3.2 \cdot 10^{19}$ cm^{-3}, boron	
d_{ox}, nm	Φ_b, eV	d_{ox}, nm	Φ_b, eV	d_{ox}, nm	Φ_b, eV
4.4	3.35	4.4	2.84	–	–
6.2	2.98			–	–
8.2	2.95	8.2	2.93	7.8	2.51

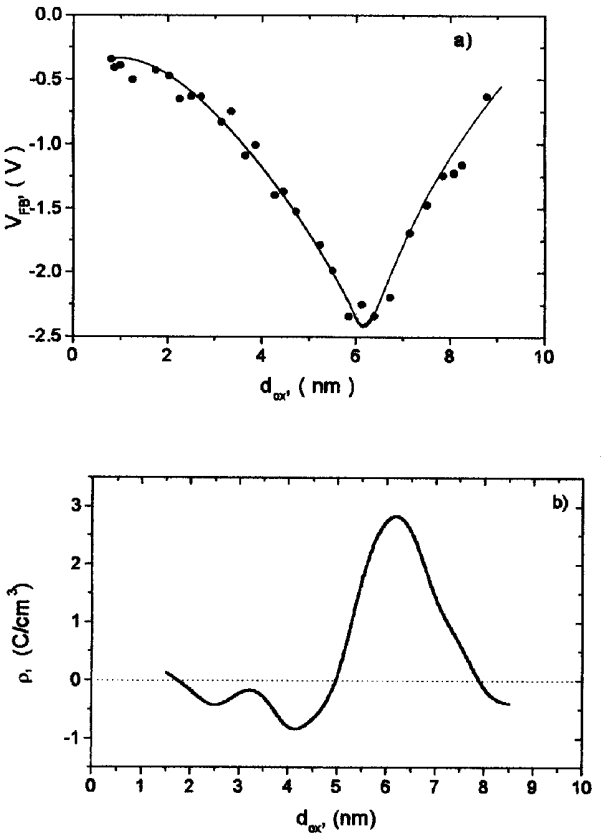

Fig. 2. Dependence of flat-band voltage on oxide thickness (*n*-Si(111), $T_{ox} = 800$ °C in dry O_2, step-by-step etching) (*a*) and distribution of built-in change in SiO_2 (*b*)

the local distribution of electric field strength and correspondingly, the current through the oxide film. The dependence of the flat band (FB) voltage (V_{FB}) on oxide thickness is obtained using step-by-step etching and shown in Fig.2,*a*. The nonuniform dependences of the flat band voltage and, correspondingly, built-in charge on oxide thickness are observed. The solution of the Poisson equation gives the density of built-in charge as

$$\rho(z) = \frac{d^2 V_{FB}}{dz^2} \frac{\varepsilon_0 \varepsilon_d}{d_{ox}}. \qquad (5)$$

As can be seen from Fig.2,*b*, the distribution of charge in silicon dioxide is nonuniform. The building of negative charge is observed near the $Si-SiO_2$ interface and in the external part of dielectric. At the central part of oxide, there is a high built-in positive charge. To take into account the influence of the built-in charge on tunneling probability at the first approximation, the whole charge localization at sites

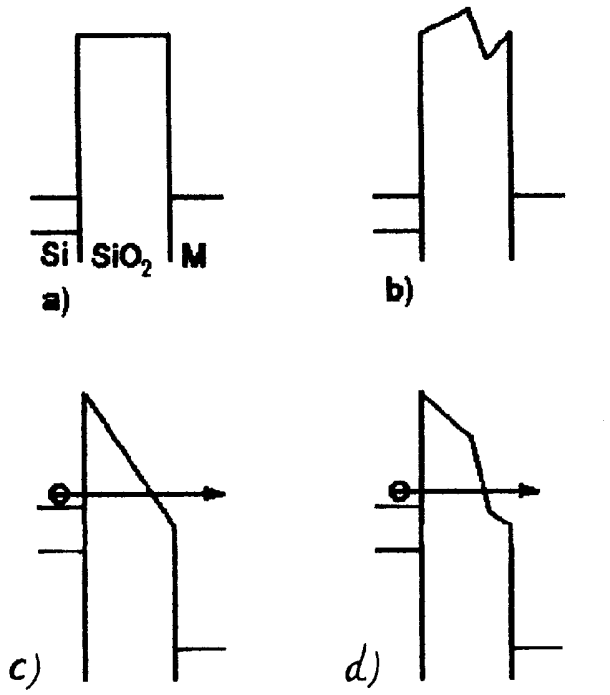

Fig. 3. Energy barriers for electrons without (*a*, *c*) and with (*b*, *d*) intrinsic electric field (*c*, *d* – at applied gate voltage)

of maximum and minima of the charge distribution curve is supposed. In this case, the energy band diagram of silicon dioxide and, correspondingly, energy barrier for electrons are, not more smooth (see Fig. 3). The estimated built-in electric fields in different parts of the barrier are as follows: $E_1 = 2.9 \cdot 10^5$ V/cm, $E_2 = 1.16 \cdot 10^6$ V/cm, $E_3 = 8.7 \cdot 10^5$ V/cm. The tunnel currents through oxide were calculated using the Fowler – Nordheim equation

$$J = A \times E^2 \exp(-B/E) = A \times E^2 \times P, \qquad (6)$$

where P is the tunneling probability.

For a complicated energy barrier, the tunneling probability was presented as the product of probabilities:

$$J = A \times E^2 \times P_1 \times P_2 \times P_3. \qquad (7)$$

The calculated Fowler – Nordheim curves without and with taking into account the intrinsic electric field are presented in Fig. 4. The experimental curves are also shown. As can be seen, the taking into account of the intrinsic electric field allows us to explain some discrepancy between experimental and theoretical curves. The second approximation which takes into account the continuous charge distribution will give

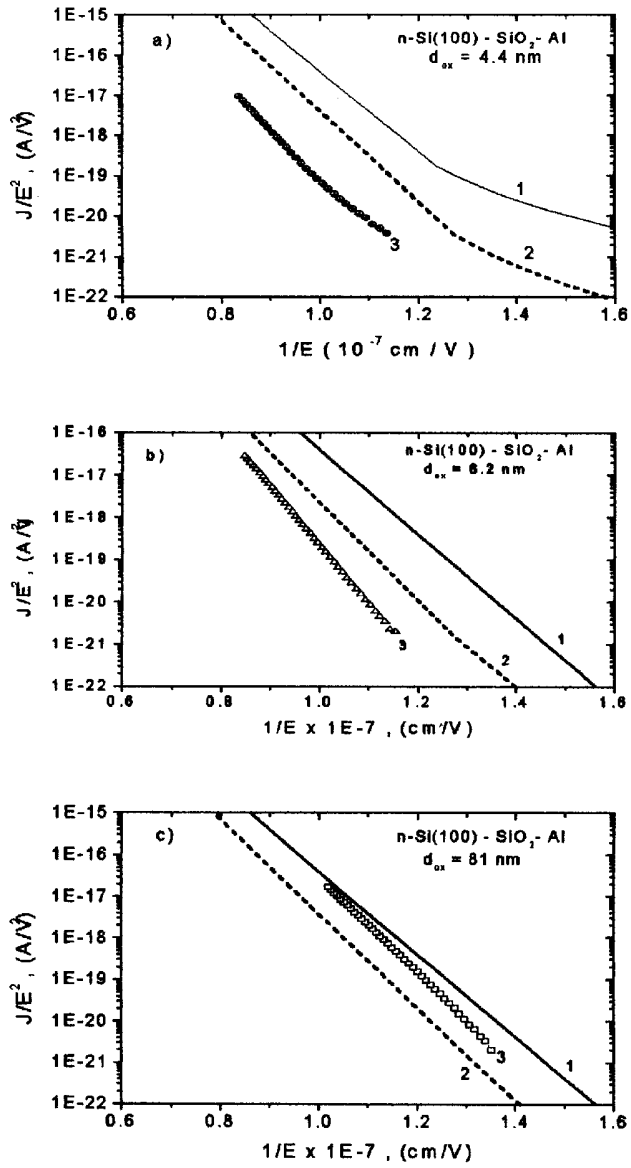

Fig. 4. Influence of build-in charge in SiO_2 on Fowler – Nordheim plots: *a* – $d_{ox} = 4.4$ nm; *b* – $d_{ox} = 6.2$ nm; *c* – $d_{ox} = 8.1$ nm (*1* – theoretical calculation without taking into account built-in charge; *2* – theoretical calculation with taking into account built-in charge; *3* – experimental data)

better agreement but, in this case, the expression for tunneling probability is too complicated.

An increase of the substrate doping level promotes the intrinsic mechanical stress relaxation due to impurities into oxide and the appearance of traps. The existence of traps can cause the tunnel current at low electric fields [5]. The possible capture of electrons in interface traps and traps in oxide near the interface prior to tunneling can occur. When the density of these

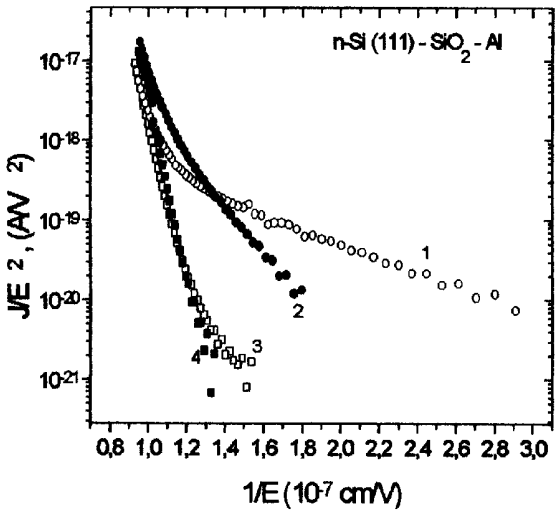

Fig. 5. Fowler – Nordheim plots of MOS structures with different SiO_2 thickness and annealing (*n*-Si): *1* – H_2O annealing, d_{ox} = 3.9 nm; *2* – H_2 annealing, d_{ox} = 3.9 nm; *3* – H_2O annealing, d_{ox} = 4.8 nm; *4* – H_2 annealing, d_{ox} = 4.8 nm

traps deep in oxide is substantial, a lowering of the Fowler – Nordheim slope would be expected due to the existence of an intrinsic electric field into SiO_2.

2.2. Influence of Annealing

To investigate the influence of annealings on the tunnel current through ultra thin SiO_2 films, silicon dioxide films were grown at 850 °C in dry oxygen. The obtained experimental results for *n*-Si are presented in Fig. 5.

The influence of annealing on tunnel current is strong and depends on the substrate type and oxide thickness. The minimum shift of the current-voltage characteristics is observed after annealing both in hydrogen and H_2O for an oxide thickness of 6.5 nm. At a higher oxide thickness, there are sufficient separations among the curves before annealing that indicates the different initial concentrations of traps at the Si–SiO_2 interface and in SiO_2. The annealing in H_2O practically removes the differences among curve positions. For thinner oxide films, the region of direct tunneling is observed. The annealing in H_2O reduces the oxide film conductivity strongly.

Conclusion

The influence of the substrate type and doping level on the electron tunnel current through SiO_2 films grown on Si is essential. This influence is dependent on oxide thickness. The annealings in H_2 and H_2O shift the current-voltage characteristics, as a rule, to the higher fields region. To explain the experimental results, the influence of charge and its distribution in SiO_2 on the experimental $I(V)$ characteristics and corresponding Fowler – Nordheim curves of the MOS structure were considered.